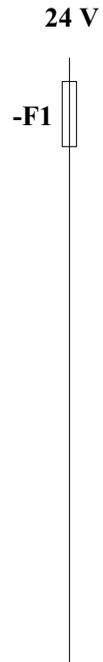
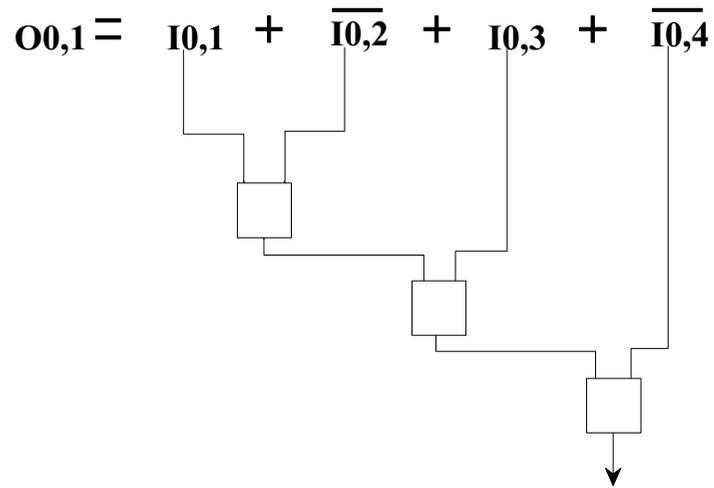
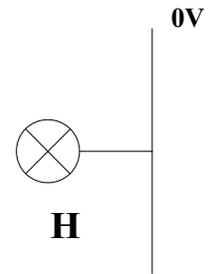


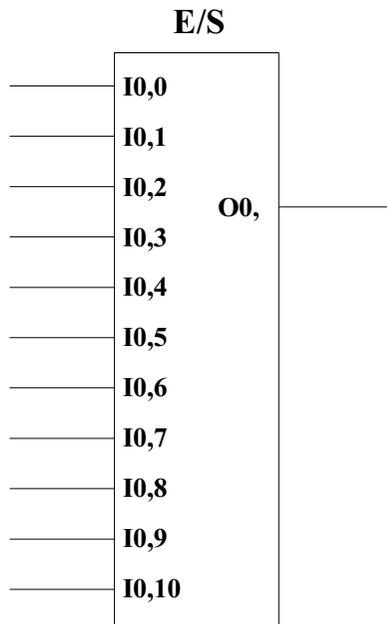
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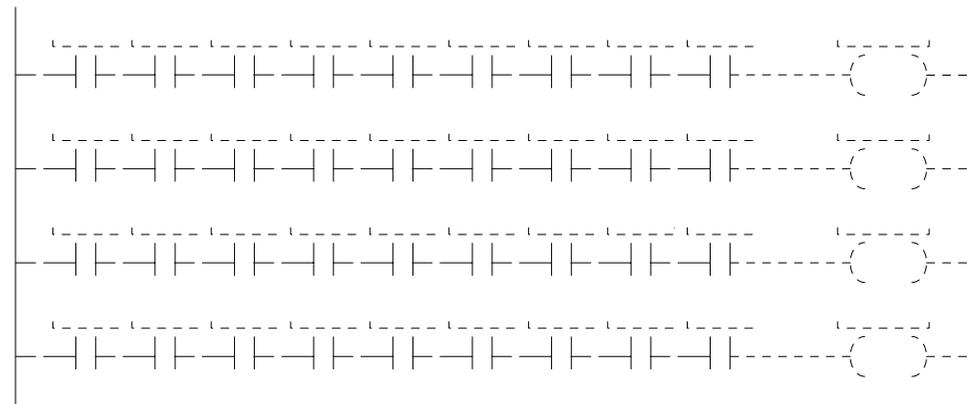
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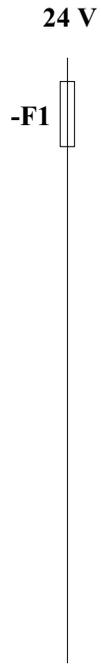
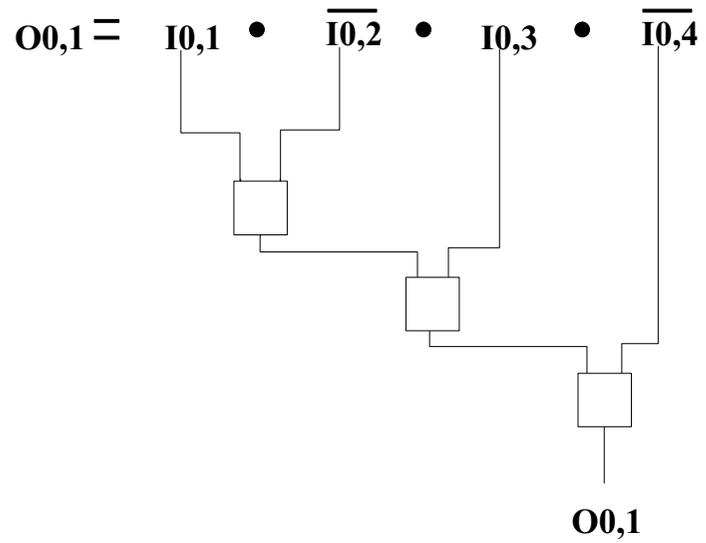
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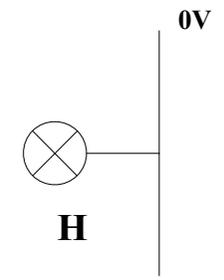
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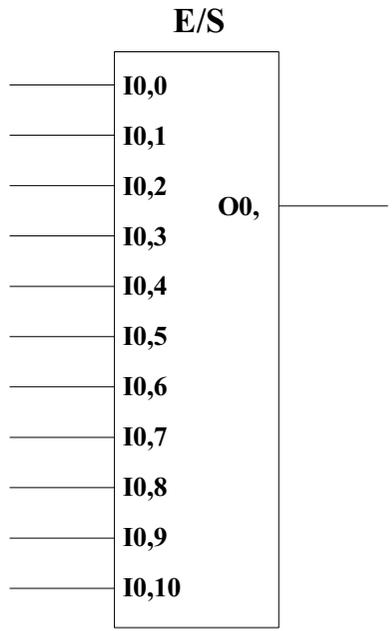
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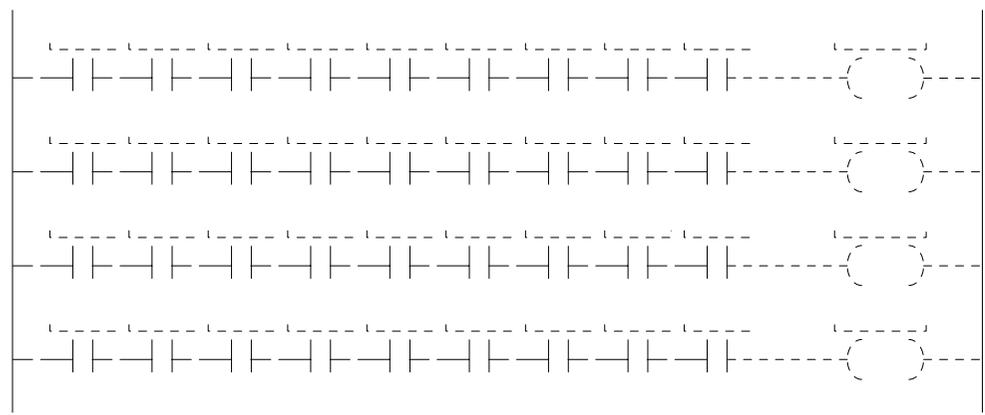
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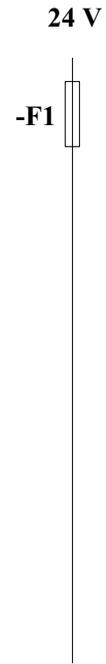
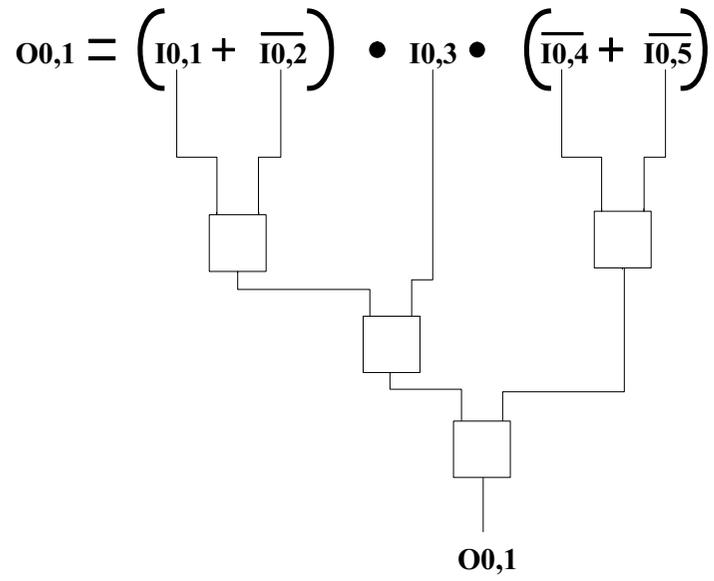
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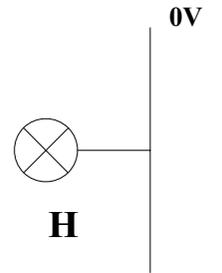
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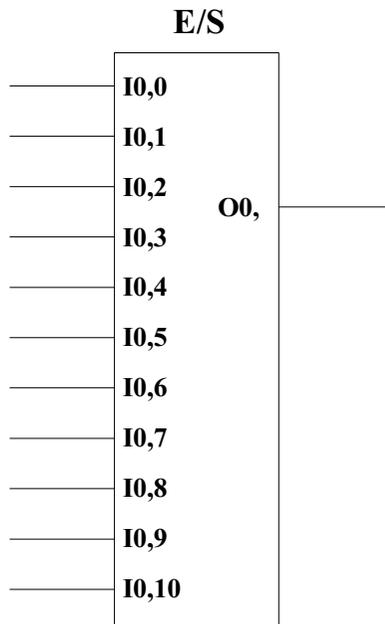
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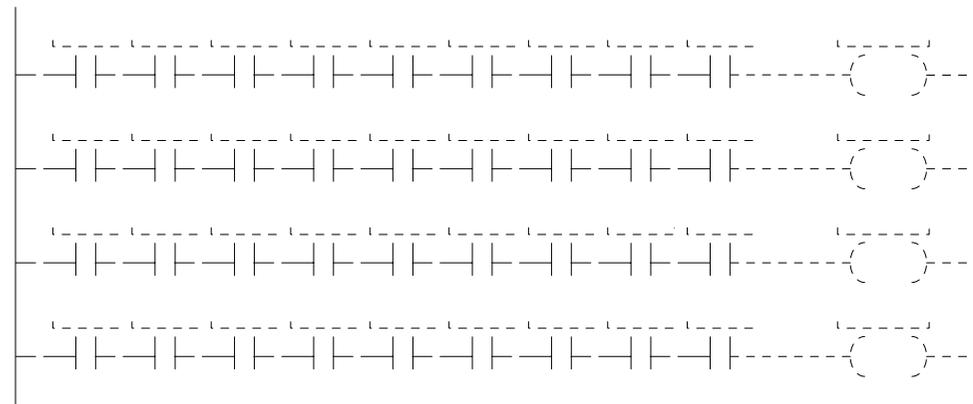
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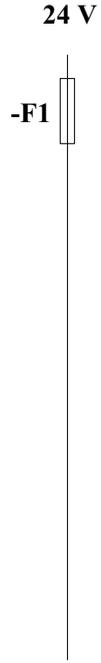
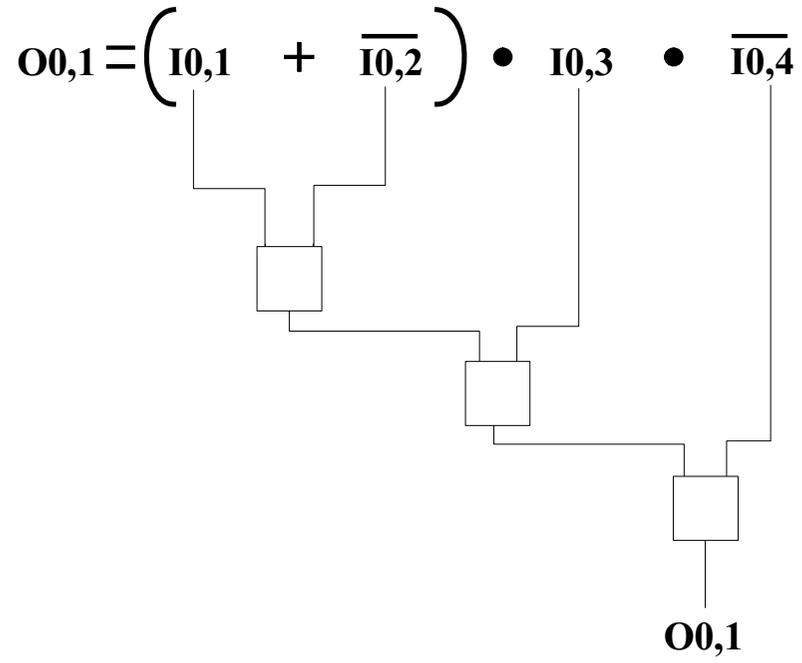
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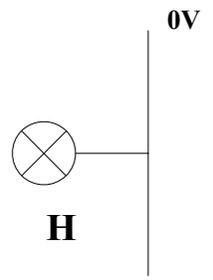
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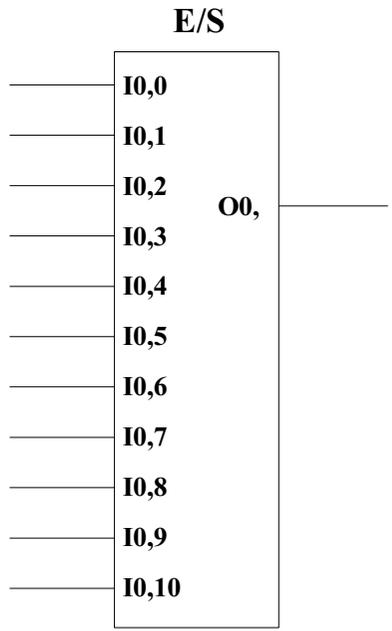
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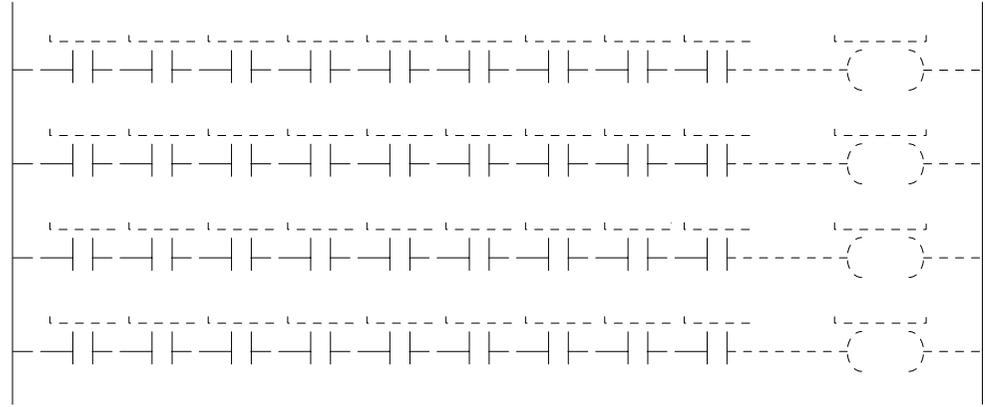
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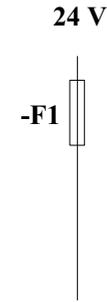
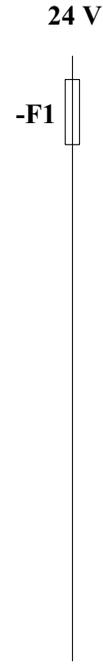
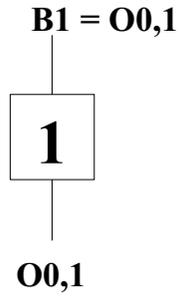
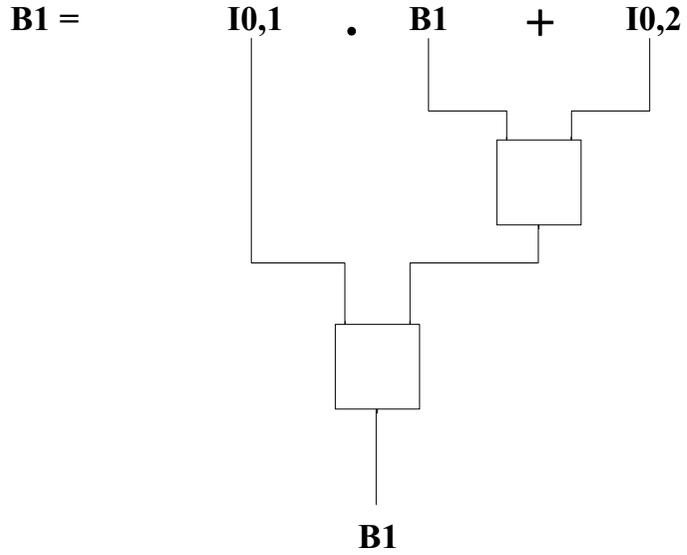
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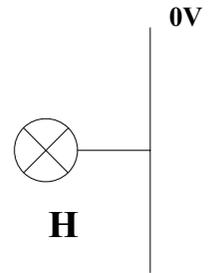
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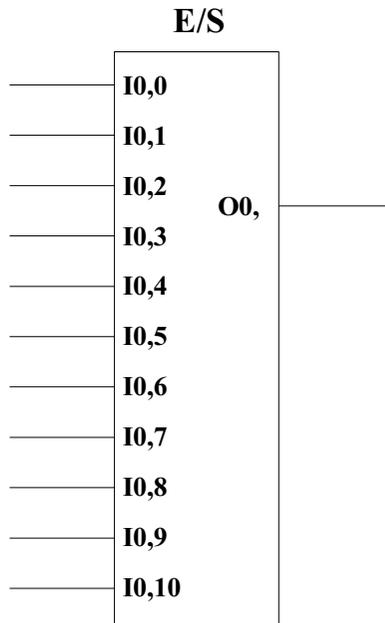
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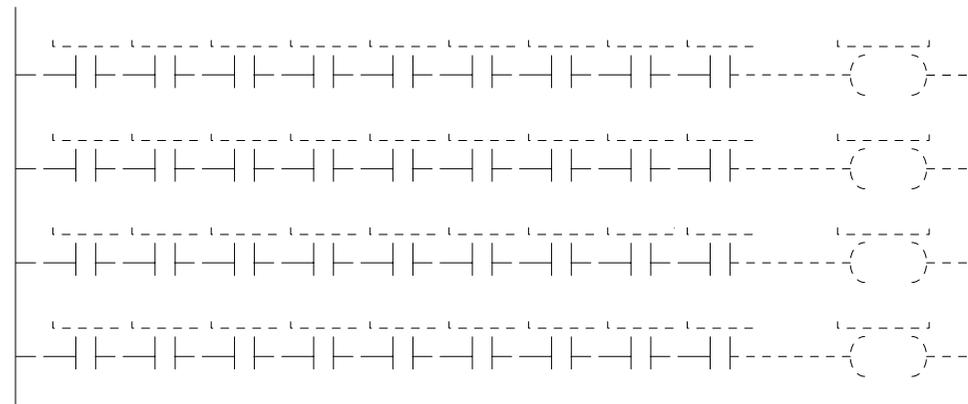
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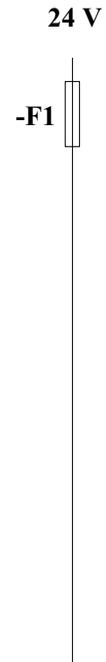
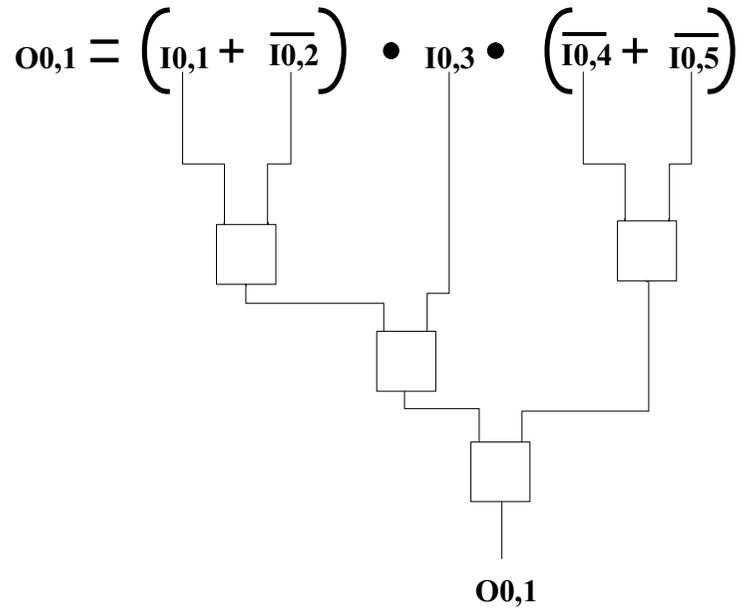
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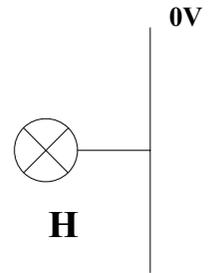
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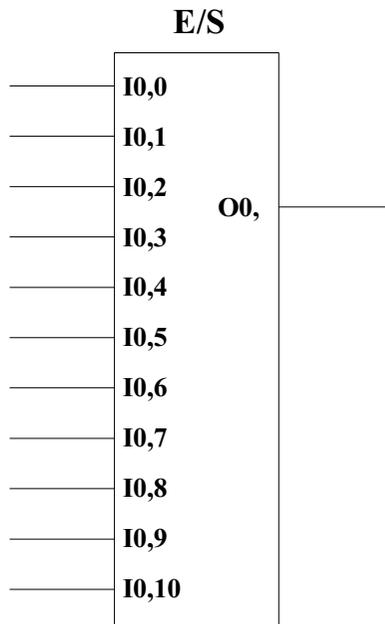
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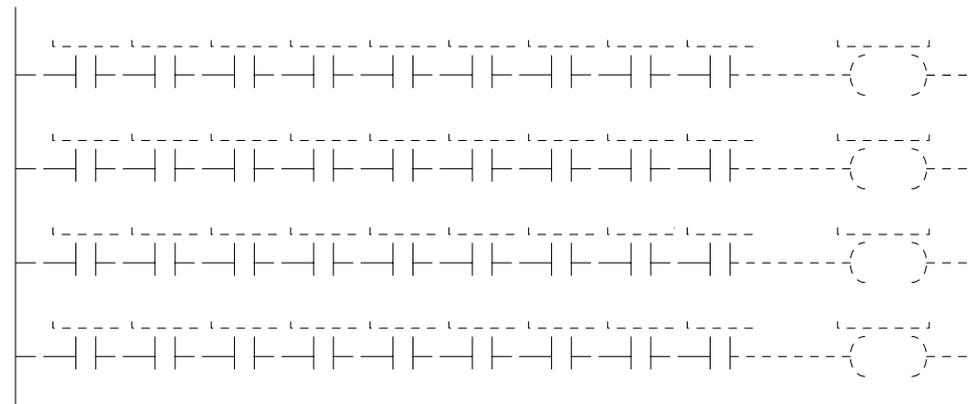
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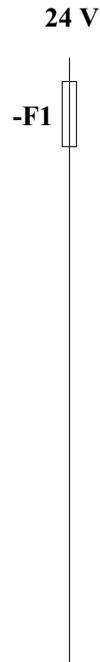
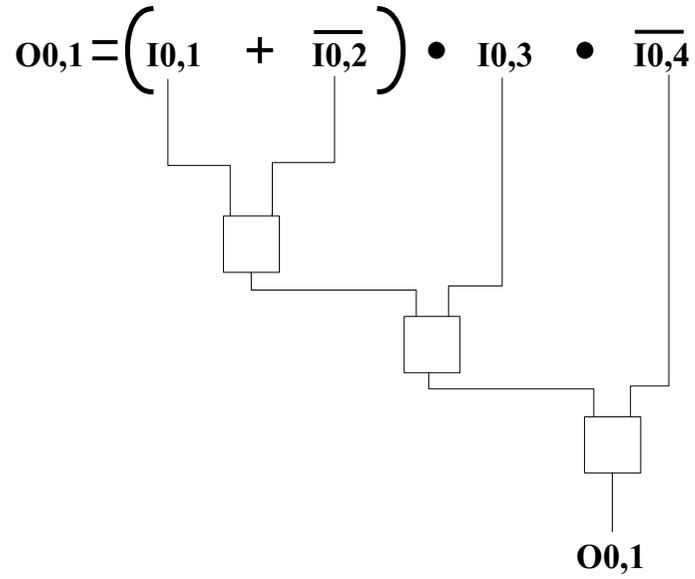
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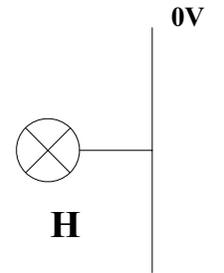
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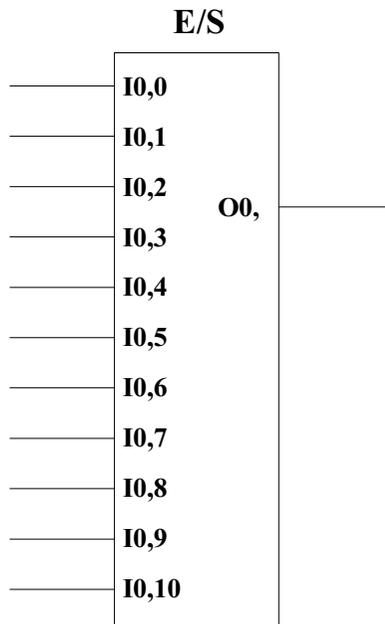
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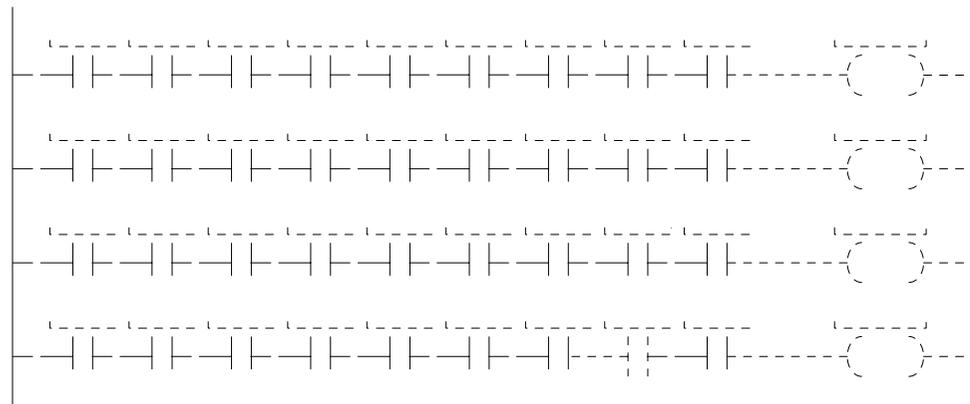
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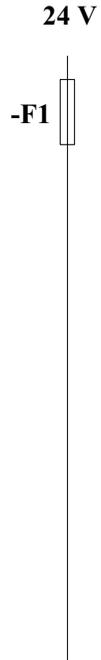
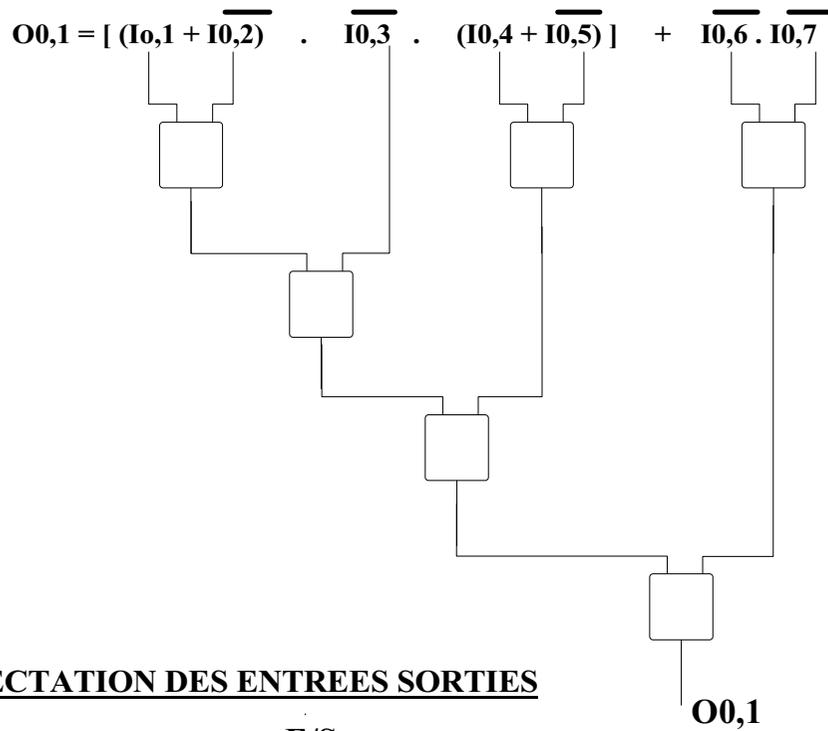
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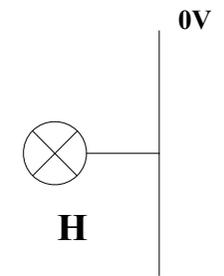
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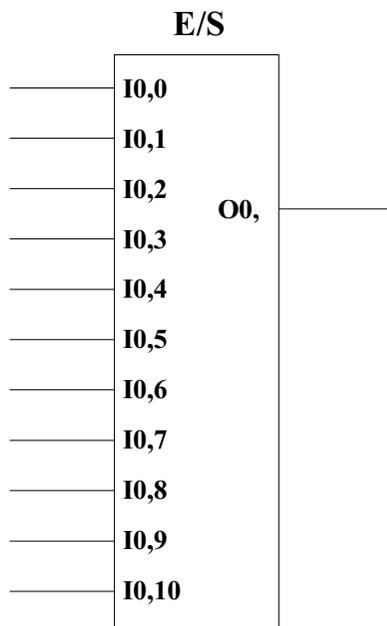
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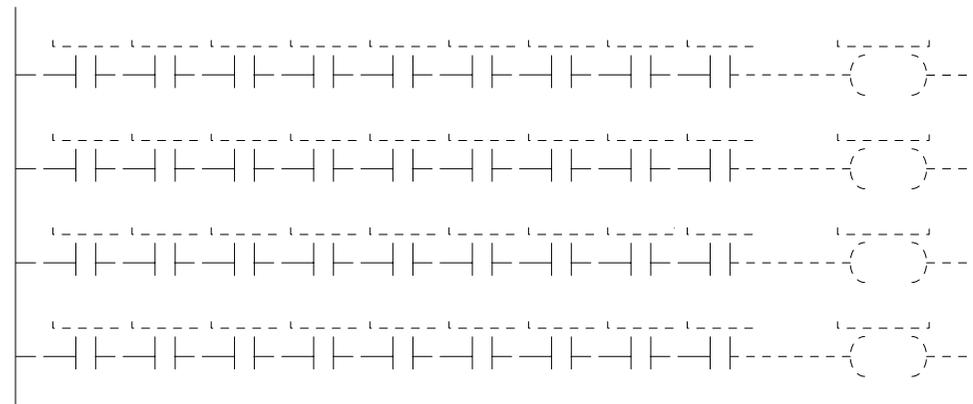
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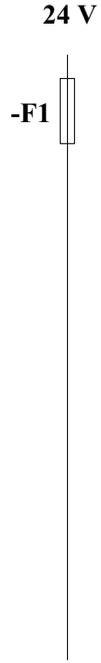
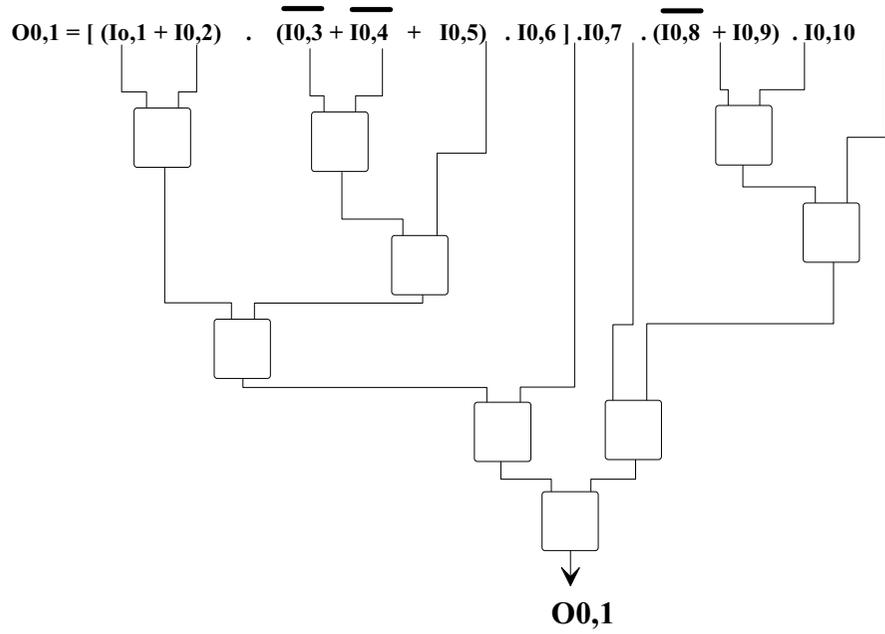
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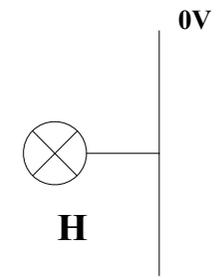
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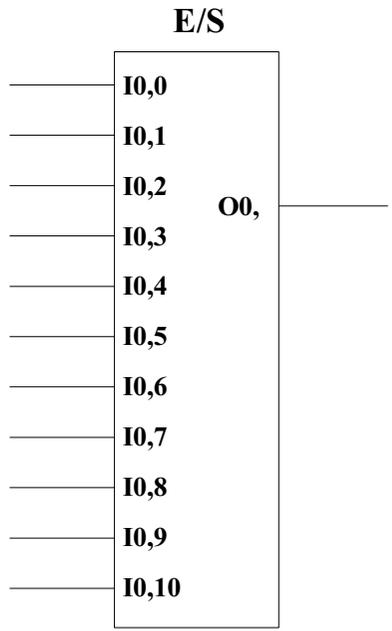
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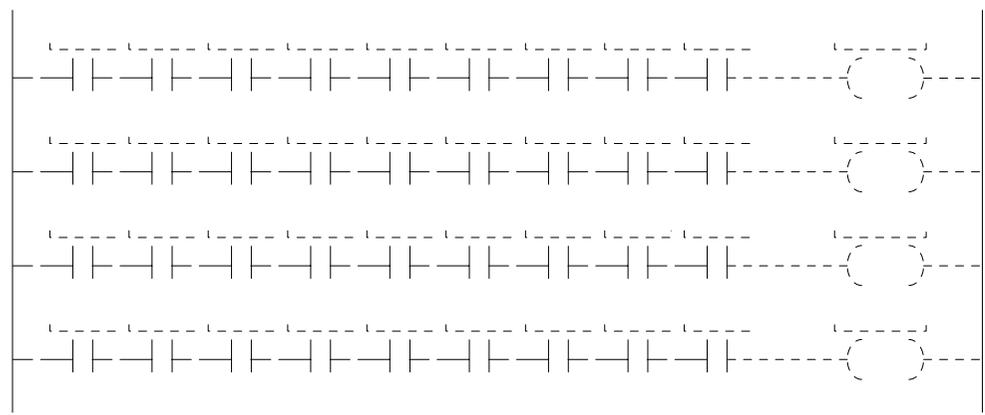
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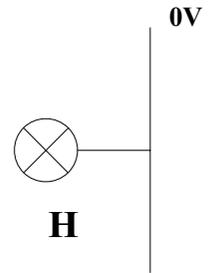


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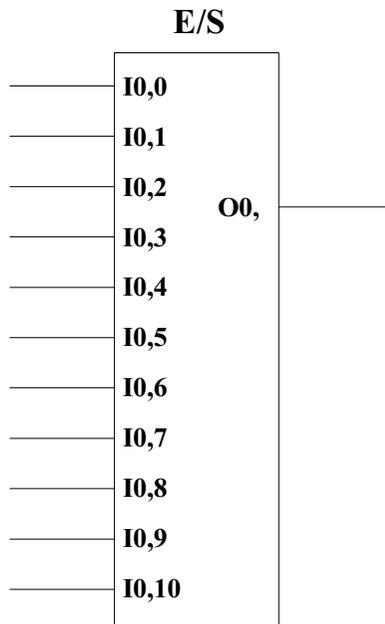


SCHEMA LOGIQUE

ELECTRIQUE



AFFECTATION DES ENTREES SORTIES



LABEL:

